18.8 A 20Gb/s Embedded Clock Transceiver in 90nm CMOS

J. Jaussi[1], B. Casper[1], M. Mansuri[1], F. O'Mahony[1], K. Canagasaby[2], J. Kennedy[1], R. Mooney[1]

[1]Intel, Hillsboro, OR
[2]Intel, Santa Clara, CA

As link data rates increase for microprocessors and backplane interfaces, operating margins continue to decrease. Data rates are limited by ISI, receiver voltage uncertainty, and clock timing uncertainty at the TX and RX. Efforts to increase performance have focused on modulation and increasingly complex forms of equalization [1, 2]. However, it is shown in this paper that for many applications, precise clocking and high sensitivity in receivers combined with a reasonable amount of equalization can enable up to 20Gb/s data rates using binary signaling. A bang-bang CDR-based architecture, with 3 taps of TX equalization and a simple RX linear equalization that enable small area and power-efficient multi-gigabit links, is described.

The TX block diagram is shown in Fig. 18.8.1. The on-die clock generator is an LC VCO PLL that provides a 10GHz clock to the TX. With passive clock distribution, the clock is buffered to drive 8 TXs. Local duty-cycle correction minimizes duty-cycle error to 1%. The binary TX has 3 taps of linear equalization. The output stage has 6 bits of resolution, consisting of binary weighted PMOS segments with poly resistor termination. The staged serializers are required to stream a 32b interface operating at 625MHz to a 1b interface operating at 20Gb/s.

Figure 18.8.2 contains the serial RX architecture that employs an LC VCO and a bang-bang phase detector (PD). In the 4-way interleaved front end, 8 comparators are required to recover data and clock with 2× oversampling. In order to achieve high sensitivities, the front end is designed with a linear source-degenerated equalizer followed by 4 samplers, 4 amplifiers, and four 5GHz offset-controlled comparators. All edge and data samples are amplified to CMOS levels and applied to the XOR phase decoder to form the PD. The PD and summer process the 4×5Gb/s data to generate the correct 5GHz phase response that drives the charge pump. The phase update rate is $^1/_4$ of the data rate. The charge pump and loop filter are implemented on-die with nominal values of 12.5µA and 73.8pF and 100Ω, respectively. For the 20Gb/s data rate, the VCO operates at 10GHz and is divided down to 5GHz and sourced to a DLL for sampling clock generation. The DLL generates the control voltage that sets the delay for the VCDL to properly space the sampling clocks for the 8 samplers and comparators. A phase interpolator also receives the 5GHz recovered clock and is used as part of the integrated on-die scope functionality [3].

The fabricated LC VCO (Fig. 18.8.3) is designed with M1 as a source follower. The gate of M1 is driven with Vbias that is referenced to V_{SS} to improve power-supply sensitivity. The cross-coupled pair, M2 and M3, generates the negative transconductance. L1 and L2 are an M7 differential spiral inductor with 52.8µm per side and have a simulated Q of 5.4 with the low resistivity substrate. The fine control has a tuning range of approximately 500MHz and the full range is ±16%. The fine tuning is controlled by Vctrl with switches in series with a capacitor. Since the Q is less than 10, this design does not further degrade the Q, and it improves power-supply sensitivity. The coarse tuning is set with the switch-capacitor bank. There are 4 capacitors to implement the coarse control with the switches and capacitors being binary weighted. This VCO is used in the TX PLL and RX CDR.

The phase summing circuit follows the XOR edge decoder and is designed as 4 tri-state inverters with each output being summed together (Fig. 18.8.4). Based on "early" or "late" phase information, the combinations of the valid edge samples generate 7 possible output voltage values from the summer: V_{CC}, $^3/_4V_{CC}$, $^2/_3V_{CC}$, $^1/_2V_{CC}$, $^1/_3V_{CC}$, $^1/_4V_{CC}$, and V_{SS}. All values above $^5/_8V_{CC}$ are considered a pump "up" and all values under $^3/_8V_{CC}$ are considered a pump "down." Any combination of the 4 phase samples that results in $^1/_2V_{CC}$ are determined to be a "don't care" and the previous state is maintained by using a Schmitt trigger. This condition only occurs when an equal number of early and late indications are received. The Schmitt trigger also helps eliminate any possible noise on the intermediate signals, $^1/_3V_{CC}$ and $^2/_3V_{CC}$. In the event that no valid edge is detected (no data transitions within the 4 data bits), the opposite pump signal of the current pump value is generated and applied to the charge pump.

The sampling clock generation is accomplished with an 8-stage DLL. The control voltage (Vctrl) from the DLL sources the VCDL shown in Fig. 18.8.4. At 20Gb/s, the VCDL is required to generate 8 sampling clock phases with 25ps of separation between sampling edges. To generate the required timing accuracy, duty-cycle correction and sampling-clock delay deskew is required. The adjustable delay range of the clock delay deskew circuit is ±6ps.

The transceiver is fabricated in a 90nm CMOS process. The measured input referred noise of the RX front end is $1mV_{rms}$. The measured closed-loop phase noise of the TX PLL at 10MHz offset with a 5GHz output is -110dBc/Hz. The VCO coarse and fine tuning ranges are shown for each of the 16 coarse capacitor settings in Fig. 18.8.3. To measure the sinusoidal jitter tolerance for the link, a bypass clock is used to clock the TX and the link is operated at 18Gb/s over a 2-inch FR4 channel while transmitting a 32b LFSR pattern. In Fig. 18.8.5, the jitter tolerance plot is shown with a BER $<10^{-12}$. Using the same measurement conditions without the sinusoidal modulation, the recovered clock is divided by 4, buffered off-chip and characterized. The measured recovered clock uncertainty showed a random jitter of $1.44ps_{rms}$ and a deterministic jitter of 1.78ps. The recovered clock spectrum is also given.

The maximum data rates when transmitting 32b LFSR pattern for 2-inch and 7-inch FR4 channels with 2 land grid array (LGA) packages and sockets are 20Gb/s and 18.85Gb/s, respectively. Maximum data rates over a backplane with 2 LGA packages and sockets, 2 FCI Airmax connectors and lengths of 15-inch and 22-inch are 16.5Gb/s and 14.4Gb/s, respectively. All maximum data-rate measurements have less than 10^{-12} BER. Figure 18.8.6 contains the paper summary and Fig. 18.8.7 shows the TX and RX micrographs.

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References:
[1] K. Yamaguchi et al., "12Gb/s Duobinary Signaling with ×2 Oversampled Edge Equalization," *ISSCC Dig. Tech. Papers*, pp. 70-71, Feb., 2005.
[2] J. Zerbe et al., "Equalization and Clock Recovery for a 2.5-10Gb/s 2-PAM/4-PAM Backplane Transceiver Cell," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2121-2130, Dec., 2003.
[3] B. Casper et al., "8Gb/s SBD Link with On-die Waveform Capture," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2111-2120, Dec., 2003.

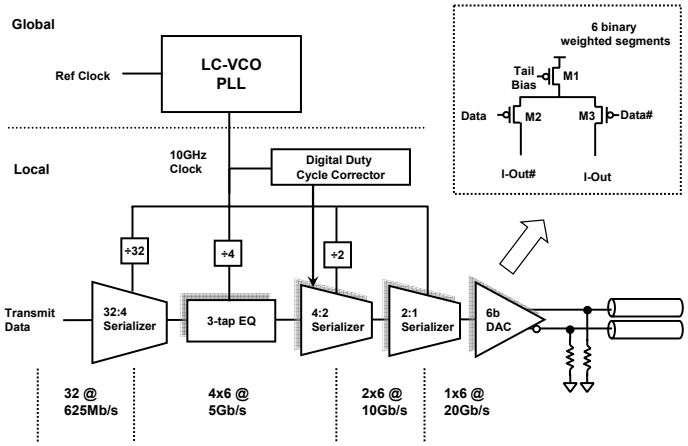

Figure 18.8.1: TX architecture.

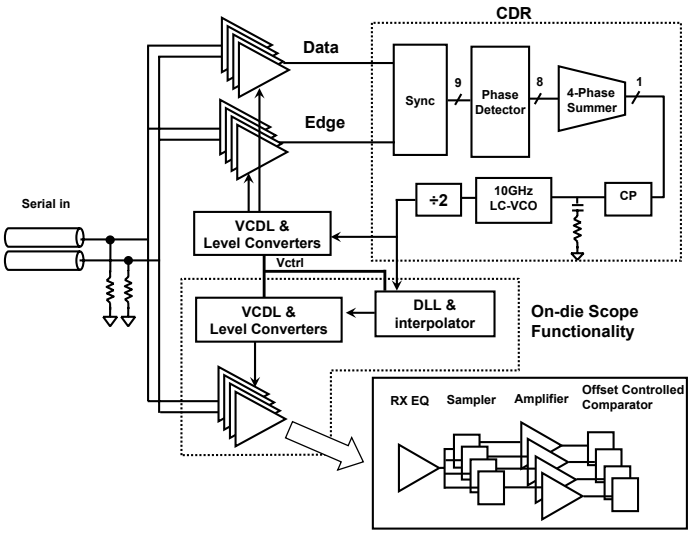

Figure 18.8.2: RX architecture.

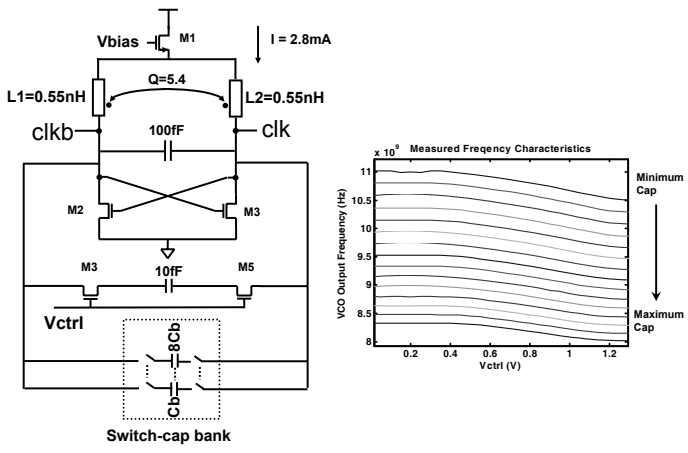

Figure 18.8.3: LC VCO circuit and measured tuning range.

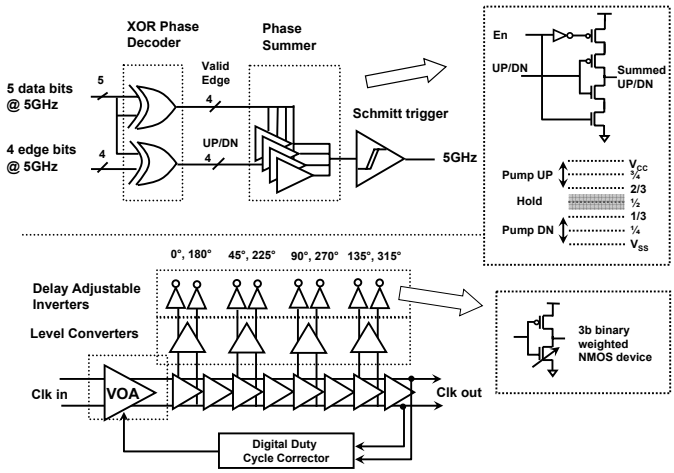

Figure 18.8.4: VCDL and duty-cycle corrector and XOR phase decoder, phase summer and Schmitt trigger circuits.

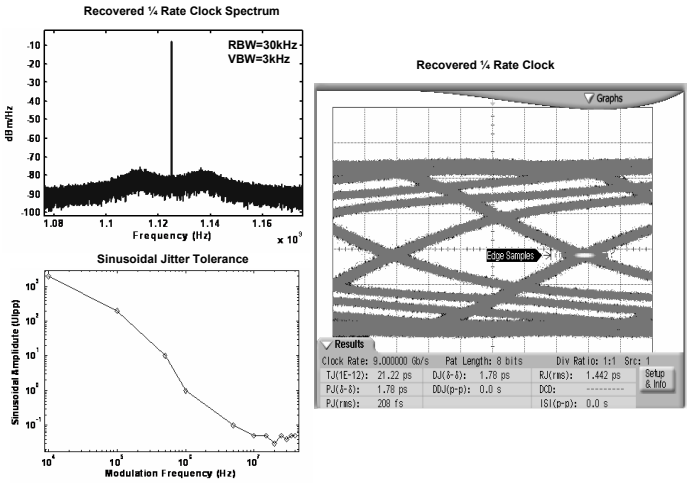

Figure 18.8.5: Measured recovered clock spectrum, measured jitter tolerance and measured recovered clock uncertainty @18Gb/s and 32b LFSR pattern.

Technology	90nm CMOS
Supply Voltage	1.2V
Maximum Data Rate (32-bit LFSR)	20Gb/s (BER <10^{-12})
Measured Power @20Gb/s (TX PLL and global clocking amortized across 8 bits)	318mW (15.9mW/Gb/s)
TX Output Voltage Swing	1V_{pp} Differential
RX Input Referred Noise	1mV_{rms}
CDR Random Jitter @18Gb/s	1.44ps_{rms}
LC VCO Tuning Range	3GHz, ±16%
I/O Cell Area	0.560mm^2

Figure 18.8.6: Test chip summary.

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18

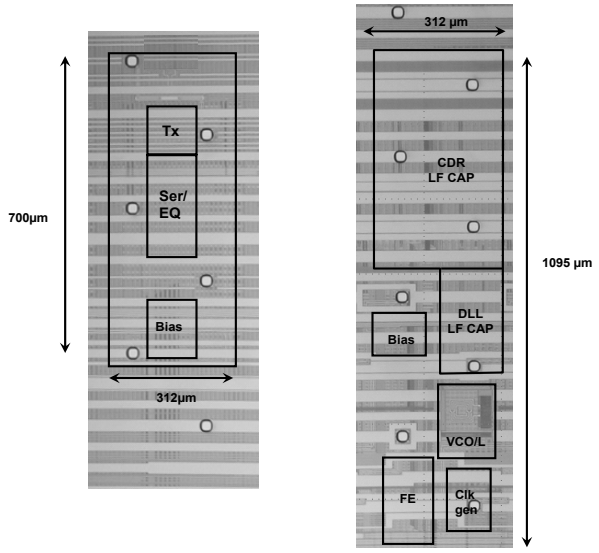

Figure 18.8.7: RX and TX micrographs.

